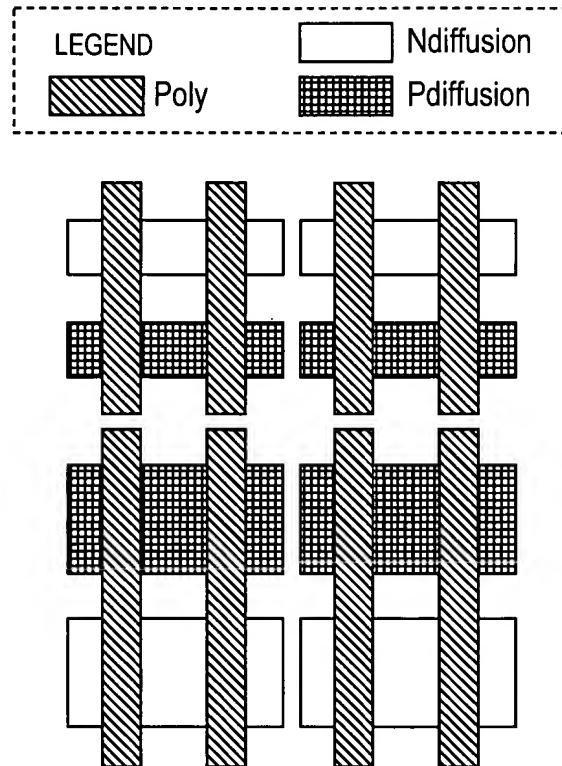




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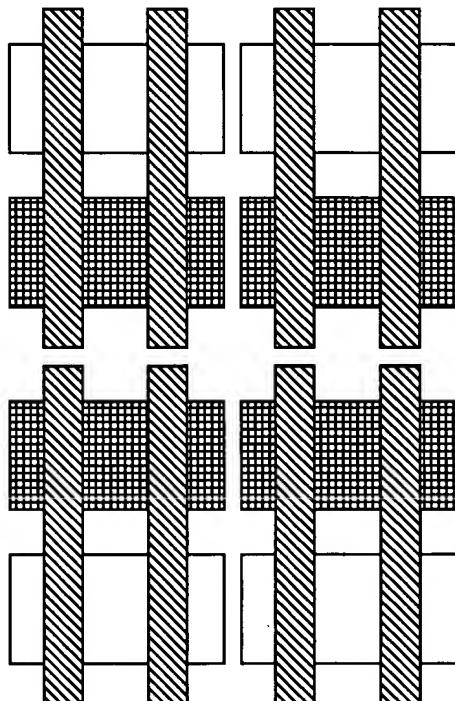
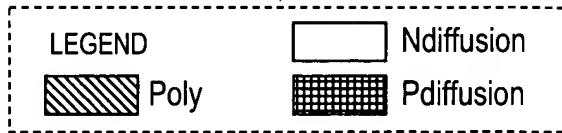
**FIG. 1**



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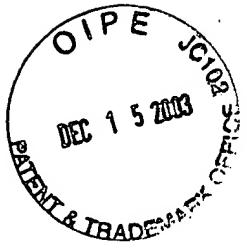
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Traditional Approach

**FIG. 2**



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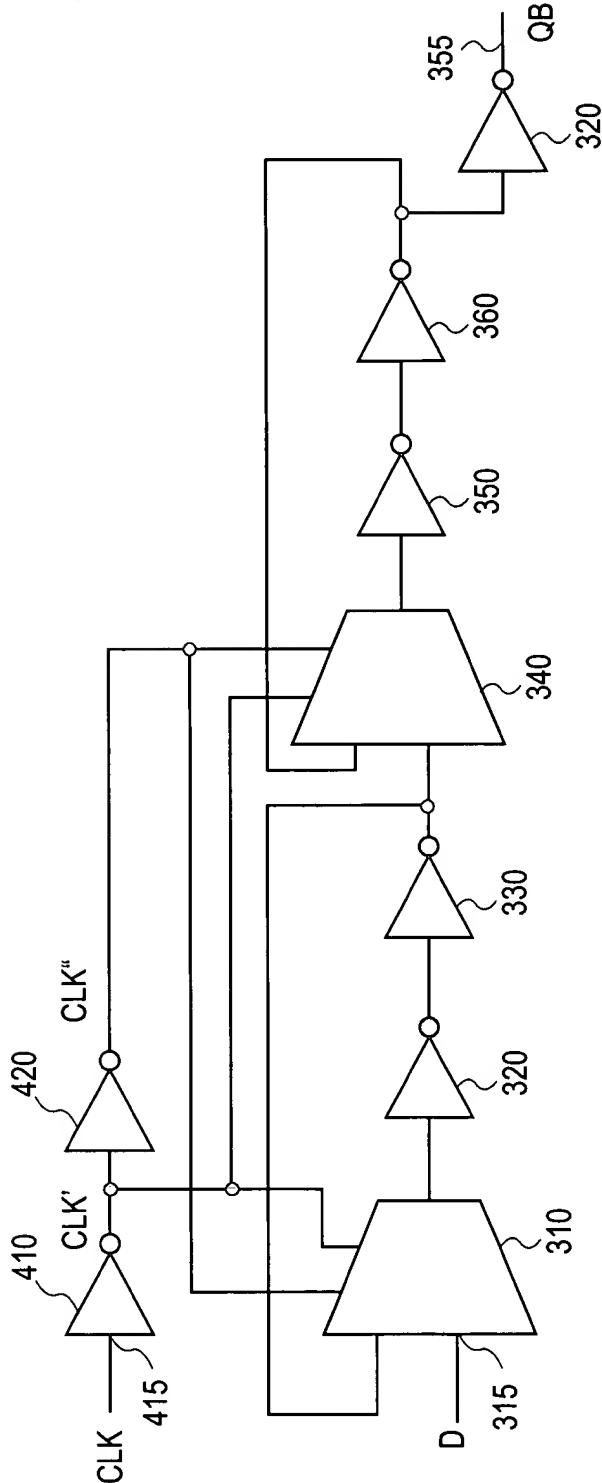
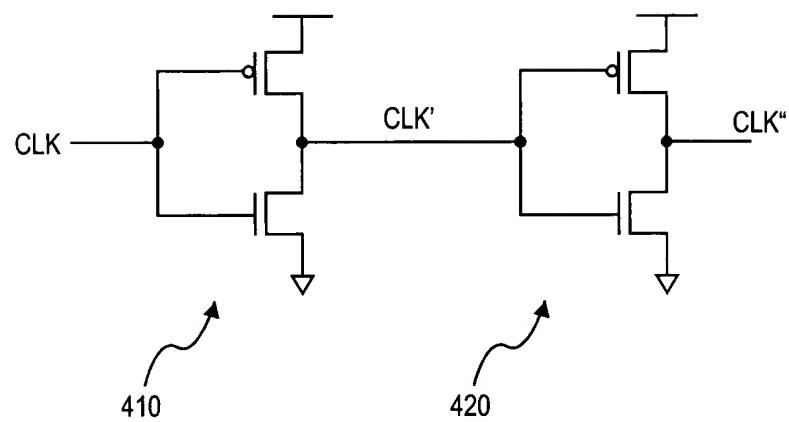


FIG. 3

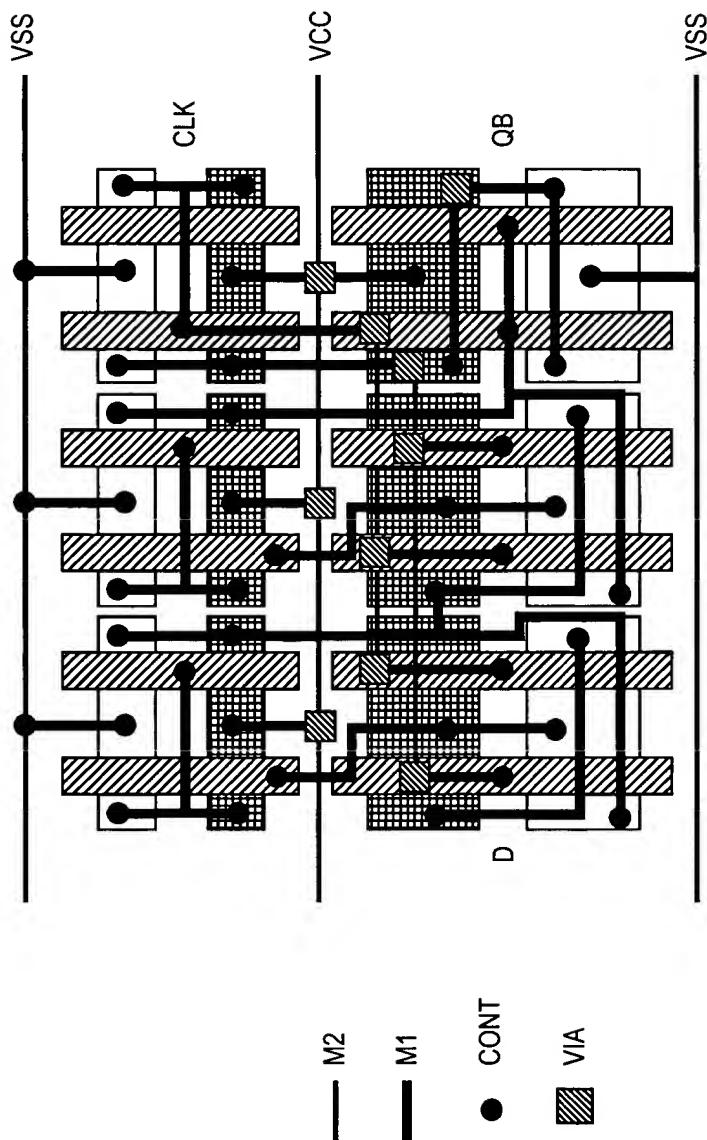


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**FIG. 4**



**FIG. 5**



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Table 1

Name	Clock Pin Power	Notes
Capacitance Improved	0.06 pJ	FIG. 2
Si Arc	0.13 pJ	SiArc CBA
Traditional	0.15 pJ	FIG. 2

pJ = pico joules

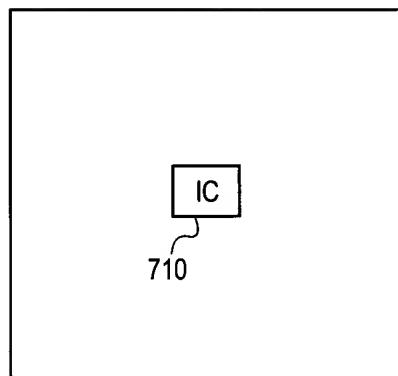
**FIG. 6**



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**FIG. 7**